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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P7178 Total Pages 5

First Named Inventor or Application Identifier John W. Horigan et al.

Express Mail Label No. EL431890268US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 15)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 2)

4. X Oath or Declaration (Total Pages 5)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ___ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ___ Computer Readable Copy
b. ___ Paper Copy (identical to computer copy)
c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. X Assignment Papers (cover sheet & documents(s))
9. ____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
____ b. Power of Attorney
10. ____ English Translation Document (if applicable)
11. ____ a. Information Disclosure Statement (IDS)/PTO-1449
____ b. Copies of IDS Citations
12. ____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. ____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. X Other: Express Certificate of Mailing

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
____ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: __

18. **Correspondence Address**
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PTO/SB/05 (12/97)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR ENCODING INFORMATION IN AN IC PACKAGE

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METHOD AND APPARATUS FOR ENCODING INFORMATION IN AN IC PACKAGE

The present invention relates to computer systems and more particularly to an IC package, such as a BGA package, that provides configuration information to the system.

BACKGROUND

Computer systems, from small handheld electronic devices to medium-sized mobile and desktop systems to large servers and workstations, are becoming increasingly pervasive in our society. Computer systems typically include one or more processors. A processor manipulates and controls the flow of data in a computer by executing instructions. To provide more powerful computer systems for consumers, processor designers strive to continually increase the operating speed of the processor. Unfortunately, as processor speed increases, the power consumed by the processor tends to increase as well.

Historically, the power consumed by the processor, and hence its speed, has been limited by two factors. First, as power consumption increases, the processor tends to run hotter, leading to thermal dissipation problems. Second, the power consumed by a processor may tax the limits of the power supply used to keep the processor operational, reducing battery life in mobile systems and diminishing reliability while increasing cost in larger systems. To combat these problems, the voltage supply level used by the processor may be reduced. Therefore, faster and more powerful processors may operate at lower voltage supply levels.

The voltage supply is typically provided to the processor through a component in the computer system called the motherboard. A motherboard is designed to accommodate a particular processor that operates at a particular voltage supply level. When a more advanced processor is introduced that operates at a lower voltage supply level, the motherboard must be redesigned to accommodate the lower voltage supply level. It can be expensive to redesign a motherboard, and this expense is passed on to the end user through the higher cost of a computer.

The present invention addresses this and other problems associated with the prior art.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, an integrated circuit (IC) package includes a substrate, a ground line, and an encoded region. The encoded region provides information based upon selective deposition of solder balls electrically coupled to the ground line.

Other features and advantages of the present invention will be apparent from the accompanying figures and the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which like references indicate similar elements and in which:

Figure 1A is a BGA package formed in accordance with an embodiment of the present invention;

Figure 1B is a cross-section of the package of Figure 1A; and

Figure 2 is the package of Figure 1A coupled to a PCB to form a component of a computer system in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

In accordance with one embodiment of the present invention, a ball grid array (BGA) package includes an integrated circuit (IC), such as a processor, in a substrate. An encoded region of the package provides information using selectively deposited solder balls in the encoded region. This information may indicate, for example, a voltage supply level for the processor.

Deposited solder balls in the encoded region are coupled to a ground line within the package. When the package is coupled to a printed circuit board (PCB), such as a motherboard, deposited solder balls in the encoded region are coupled to a power supply via resistors and a power trace on the motherboard. In this manner, the presence or absence of a solder ball in the encoded region can be sensed by the motherboard. Thus, the information is automatically provided to the system to properly configure the voltage supply level to the processor.

In accordance with an embodiment of the present invention, a single motherboard can be designed that accommodates various processors requiring different voltage supply levels. The proper voltage supply level is indicated to the motherboard by selective deposition of solder balls in the encoded region of the

processor package in the manner described above. Thus, system cost is reduced because there is no need to design different motherboards for each different processor. A single, mass-produced motherboard may be used. A more detailed description of embodiments of the present invention, including various configurations and implementations, is provided below.

Figure 1A is a BGA package, 100, formed in accordance with an embodiment of the present invention. As used herein, a BGA package is intended to refer to any IC package that includes I/O, power, or ground ports formed of electrically conductive balls that are deposited onto a substrate in any pattern through a template. Electrically conductive balls are herein referred to as solder balls, and include not only electrically conductive balls but also electrically conductive bumps, cylinders, parallelepipeds, ellipsoids, or any other electrically conductive shape.

BGA package 100 of Figure 1A includes substrate 101 and solder balls 102. Note that to avoid obscuring Figure 1A, reference numeral 102 only points to 4 of the numerous solder balls shown. Substrate 101 includes one or more ICs (not shown) having I/O, power, or ground pads that are electrically coupled to solder balls 102. In accordance with one embodiment of the present invention, substrate 101 includes a processor.

The surface of substrate 101 of BGA package 100 of Figure 1A may include an electrically insulative (dielectric) material, such as plastic or ceramic. Onto this surface, solder balls 102 may be screen printed. This screening process includes screen printing solder, or another electrically conductive material, through a template (or "screen") that has openings adjacent to portions of the substrate where

solder balls are deposited. Solder balls are prevented from being deposited on portions of the substrate adjacent to closures in the template. For an alternate embodiment of the present invention, solder balls are deposited on the substrate of a BGA package through a template by a process other than screening such as, for example, chemical vapor deposition and sputtering.

The ease and economy with which the solder ball pattern on a BGA package can be modified makes embodiments of the present invention advantageous over, for example, IC redesign, IC pad bond-out, or internal package redesigns. Templates used to form alternate solder ball patterns on a BGA package can be relatively cheaply and quickly produced. Thus, information specific to a particular BGA package (and, more particularly, specific to the IC contained within the package) may be cheaply and easily encoded by the selective deposition of solder balls using package-specific templates.

BGA package 100 of Figure 1A includes encoded region 105. For the embodiment shown, encoded region 105 includes five solder ball areas 111, 112, 113, 114, and 115. Each of these solder ball areas may or may not include a solder ball, depending on the information one desires to encode. For the embodiment of Figure 1A, solder balls are shown deposited in solder ball areas 111, 113, and 115, and solder balls are absent from solder ball areas 112 and 114. If a solder ball is deposited in a solder ball area of the encoded region, it denotes one logic level, and the absence of a solder ball from the solder ball area denotes the opposite logic level.

Thus, the solder ball pattern in encoded region 105 of Figure 1A denotes the five bit binary number "01010" assuming that a deposited solder ball denotes a logical "0" and that the bits are to be read linearly within the encoded region. For an alternate embodiment of the present invention, a deposited solder ball denotes a logical "1", in which case the solder ball pattern in encoded region 105 denotes the five bit binary number "10101", still assuming that the bits are to be read linearly. Alternatively, the bits may be read non-linearly according to a predefined sequence.

According to an embodiment of the present invention, the encoded region of a BGA package is a predefined region that provides information based upon the selective deposition of solder balls in the region. The region may encompass any number of solder ball areas that may or may not be adjacent to one another. The information may be provided visually to either a human observer or to an optical scanner. Alternatively, the information may be provided to a PCB to which the BGA package is coupled, as described below. The information may indicate, for example, a voltage supply level to be provided to the IC in the BGA package, a clock frequency, or other configuration information.

Figure 1B is a cross-section of the package of Figure 1A through encoded region 105. As shown, substrate 101 of BGA package 100 includes a ground line 107 to which solder ball 110 is electrically coupled. In addition, any solder balls deposited in solder ball areas 111-115 of encoded region 105, such as the solder balls in solder ball areas 111, 113, and 115, are coupled to ground line 107. A ground line is an electrical interconnect that is to be electrically coupled to ground during operation of the IC within the BGA package. Ground line 107 is electrically

coupled to ground via solder ball 110 as described below in conjunction with Figure 2. One type of ground line is a ground plane.

For an alternate embodiment of the present invention, any solder balls deposited in the solder ball areas of an encoded region of a BGA package are coupled to a power line. A power line is an electrical interconnect that is to be electrically coupled to a voltage (or power) supply, such as Vcc, during operation of the IC within the BGA package. One type of power line is a power plane. For an embodiment in which selectively deposited solder balls in an encoded region of a BGA package are electrically coupled to a power line, the circuit of Figure 2 may be appropriately modified to electrically determine the presence or absence of solder balls in solder ball areas of the encoded region.

Figure 2 is the package of Figure 1A coupled to PCB 200 to form a component of a computer system in accordance with an embodiment of the present invention. PCB 200 may be the motherboard of the computer system. The electrical interconnects that are shown outside of BGA package 100 in Figure 2 are actually traces that may be formed on or in PCB 200.

PCB 200 of Figure 2 includes ground trace 210 electrically coupled to solder ball 110. Ground trace 210 is electrically coupled to ground during operation of the computer system. PCB 200 further includes traces 211, 212, 213, 214, and 215 electrically coupled to any solder balls deposited in solder ball areas 111, 112, 113, 114, and 115, respectively. For example, for the embodiment shown in Figure 2, the solder ball deposited in solder ball area 111 of encoded region 105 is electrically coupled to trace 211. The solder ball deposited in solder ball area 113 is electrically

coupled to trace 213. The solder ball deposited in solder ball area 115 is electrically coupled to trace 215.

Each of traces 211-215 of Figure 2 is coupled to a node of a resistor disposed on PCB 200, one resistor per trace. The other nodes of the resistors are coupled to power trace 216 formed on PCB 200. Power trace 216 is electrically coupled to a voltage (or power) supply, such as Vcc, during operation of the computer system.

When a voltage is supplied to power trace 216 and ground trace 210 is grounded, the voltage levels on traces 211-215 of Figure 2 indicate the presence or absence of a solder ball in a solder ball area of encoded region 105. These voltage levels denote the logical levels of the binary information provided from BGA package 100 to PCB 200 based on the selective deposition of solder balls in the encoded region. For example, during operation, the voltage on traces 211, 213, and 215 is approximately ground, and the voltage on traces 212 and 214 is approximately Vcc. Thus, as stated above, the binary number 01010 is denoted by the solder ball pattern in encoded region 105, assuming positive logic is used and the bits are to be read linearly within the encoded region.

This binary number may be used by PCB 200 of Figure 2, or any other component of the computer system, to, for example, properly configure a voltage supply level provided to the IC within BGA package 100. Alternatively, the information may be used to, for example, properly configure another IC within the computer system to operate at the proper bus speed to enable communication with the IC within BGA package 100.

This invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident to persons having the benefit of this disclosure that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An integrated circuit (IC) package comprising:

a substrate including an IC;

a ground line; and

an encoded region to provide information based upon selective deposition of solder balls electrically coupled to the ground line.

2. The package of claim 1, wherein the substrate is the substrate of a ball grid array (BGA) package.

3. The package of claim 2, wherein the IC is a processor.

4. The package of claim 3, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

5. The package of claim 4, wherein the encoded region includes at least three solder ball areas.

6. The package of claim 5, wherein the information indicates a voltage supply level for the IC.

7. The package of claim 1, wherein the information indicates a voltage supply level for the IC.

8. An electronic component comprising:

a ball grid array (BGA) package including an encoded region to provide information based upon selective deposition of solder balls; and

a printed circuit board (PCB) coupled to the package.

9. The component of claim 8, wherein the BGA package contains a processor.

10. The package of claim 9, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".

11. The package of claim 8, wherein any deposited solder ball in a solder ball area of the encoded region is electrically coupled to a first node of a resistor on the PCB, and a second node of the resistor is electrically coupled to a power trace on the PCB.

12. The package of claim 11, wherein the first node is approximately ground if a solder ball is deposited in the solder ball area, and the first node is approximately Vcc if a solder ball is absent from the solder ball area.

13. The package of claim 12, wherein the encoded region includes at least three solder ball areas.

14. The package of claim 13, wherein the information indicates a voltage supply level for a processor within the BGA package.

15. A method of encoding information in an integrated circuit (IC) package, the method comprising:

depositing a first solder ball in a first solder ball area of an encoded region of an IC package to denote a first logical level; and

preventing a solder ball from being deposited in a second solder ball area of the encoded region of the IC package to denote a second logical level.

16. The method of claim 15, wherein depositing the solder ball includes screen printing solder through a template comprising an opening adjacent to the first solder ball area, and preventing a solder ball from being deposited includes screen printing solder through a template comprising a closure adjacent to the second solder ball area,

17. The method of claim 15, further comprising depositing a second solder ball in a third solder ball area of the encoded region of the IC package to denote the first logical level.

18. The method of claim 15, further comprising preventing a solder ball from being deposited in a fourth solder ball area of the encoded region of the IC package to denote the second logical level.

ABSTRACT OF THE DISCLOSURE

An integrated circuit (IC) package includes a substrate, a ground line, and an encoded region. The encoded region provides information based upon selective deposition of solder balls electrically coupled to the ground line.

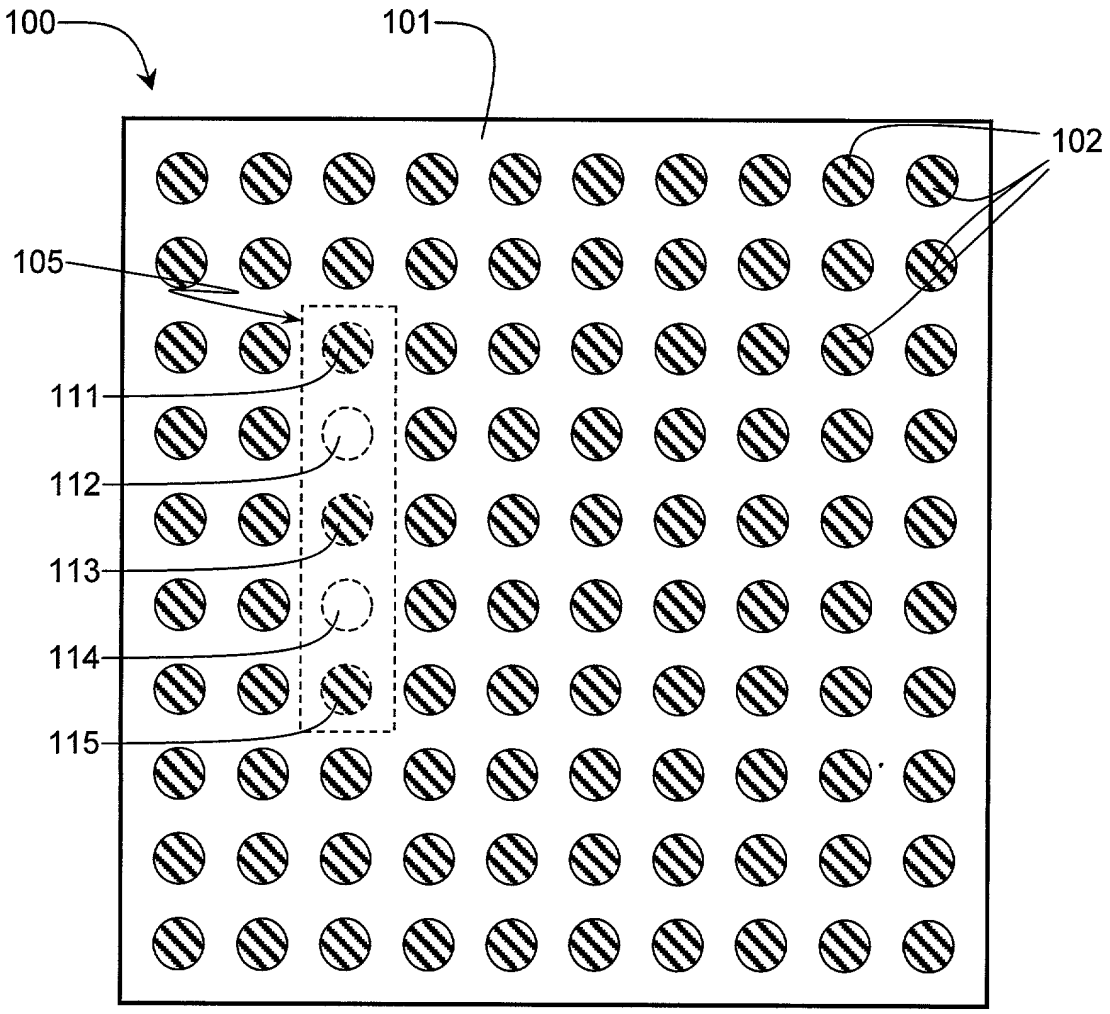

Figure 1A

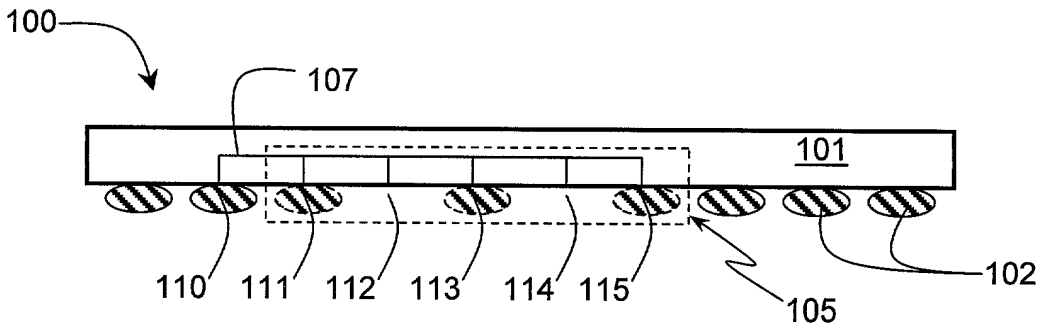

Figure 1B

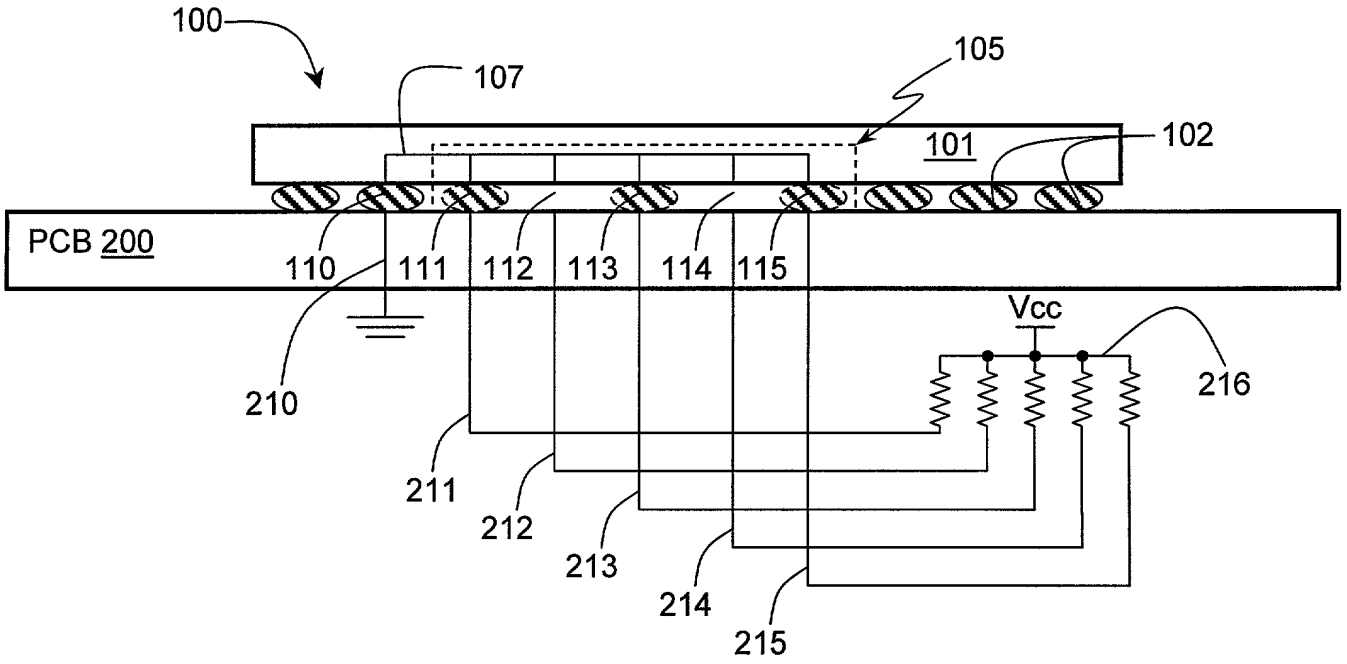
100
107
105
101
102
PCB 200
110
111
112
113
114
115
Vcc
216
210
211
212
213
214
215

Figure 2

Attorney's Docket No.: 042390.P7178 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
METHOD AND APPARATUS FOR ENCODING INFORMATION IN AN IC PACKAGE

the specification of which

__X__ is attached hereto.
_____ was filed on _____ as United States Application Number _____ or PCT International Application Number_____ and was amended on _____. (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to David Kaplan, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to David Kaplan, (408) 765-1823.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature John W. Horigan Date 12/15/99

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.